

DEC. 13. 2005 12:37PM SYNOPSYS INC

NO. 688 P. 2/3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/760,063
Filed : 01/12/01
Inventors : Kevin M. Harer, Pei-Hsin Ho and Robert F. Damiano
Title : SIMULATION-BASED FUNCTIONAL VERIFICATION OF
MICROCIRCUIT DESIGNS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.132 DECLARATION OF ROBERT F. DAMIANO

I, Robert F. Damiano, being duly warned that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent resulting therefrom, declare that:

1. The term "Ho et al." shall be used in this Declaration to refer to the following publication: P. Ho, T. Shiple, K. Harer, J. Kukula, R. Damiano, V. Bertacco, J. Taylor and J. Long. Smart Simulation Using Collaborative Formal and Simulation Engines. In ICCAD, 2000, pp. 120-126.
2. Section 3 (entitled "Unreachability") of Ho et al. only describes techniques for performing unreachability analysis.
3. T. Shiple, J. Kukula, V. Bertacco, J. Taylor and J. Long would not be included as authors of Ho et al. if Ho et al. did not include section 3.
4. For the above-referenced patent application, unreachability analysis is presented as an optional module to increase the efficiency of the formal search. Please see, for example, page 24 of the application at lines 2-5.

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5. No claim of the above-referenced patent application distinguishes between the techniques of section 3 of Ho et al. and prior art approaches to unreachability analysis.
6. In this Declaration, all statements made of my own knowledge are true, and all statements made on information and belief are believed to be true.

Dated:

12/13/05
(mm/dd/yy)

By:

Robert F. Damiano
Robert F. Damiano